**CHAPTER 3**

**EXPERIMENTATION**

This chapter includes the experimentation; the frequency division logic development process has been described in detail. The results from the experimentation are also described and the simulation outputs are specified.

**3.1 VLSI Hardware Descriptive Code**

The algorithm of the frequency division logic is as follows-

**Step 1:** Start.

**Step 2:** Accept the input clock and the reset value.

**Step 3:** Check if the reset signal is 1, if yes then jump to step 4, otherwise step to step 5.

**Step 4:** Reset the inbuilt counter and the inbuilt clock generating signal. Jump to step

3.

**Step 5:** Initialize the counter from 0 and check if counter has reached the value (Dividing

Factor \* (100 – Duty Cycle)/100). If yes jump to step 6 otherwise if counter value is (Dividing Factor) jump to step 7 otherwise, jump to step 8.

**Step 6:** Change the value of inbuilt clock signal and increment counter, jump to step 5.

**Step 7:** Change the value of inbuilt clock signal and increment counter, jump to step 5.

**Step 8:** Increment counter, jump to step 5.

**Step 9:** The output is the value inbuilt clock signal.

**End**

entity freqdiv11 is

Port (

clk\_in: in STD\_LOGIC;

reset : in STD\_LOGIC;

clk\_out: out STD\_LOGIC

);

end freqdiv11;

* 1. **Test-bench**

The test bench of the above mentioned code basically involves applying a 50MHz clock supply to the input of the FPGA. The test bench is also written in the same Xilinx model.

The test bench involves, creating a clock signal input using the wait command and setting the value of the clock signal to active high and low after recurring time intervals

In the recurring process in the test bench. The test bench is fairly simple as the clock signal is applied internally and this is a logical clock signal.

The logical part of the clock signal can be described as follows-

Clock is set to 1

Wait for 20 nanoseconds.

Clock is set to 0

Wait for 20 nanoseconds.

* 1. **Synthesis Report and RTL schematic**

This sub-chapter includes the report obtained from the experimentation.

**Synthesis Report**

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\* Final Report \*

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Final Results

RTL Top Level Output File Name : freqdiv11.ngr

Top Level Output File Name : freqdiv11

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Design Statistics

# IOs : 3

Macro Statistics :

# Registers : 2

# 1-bit register : 1

# 18-bit register : 1

# Multiplexers : 1

# 2-to-1 multiplexer : 1

# Adders/Subtractors : 1

# 18-bit adder : 1

Cell Usage :

# BELS : 81

# GND : 1

# LUT1 : 18

# LUT2 : 1

# LUT2\_L : 1

# LUT3\_L : 15

# LUT4 : 5

# LUT4\_D : 1

# LUT4\_L : 4

# MUXCY : 17

# VCC : 1

# XORCY : 17

# FlipFlops/Latches : 19

# FDC : 19

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 2

# IBUF : 1

# OBUF : 1

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Device utilization summary:

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Selected Device : 3s200pq208-5

Number of Slices: 25 out of 1920 1%

Number of Slice Flip Flops: 19 out of 3840 0%

Number of 4 input LUTs: 45 out of 3840 1%

Number of bonded IOBs: 2 out of 141 1%

Number of GCLKs: 1 out of 8 12%

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TIMING REPORT

Clock Information:

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Clock Signal | Clock buffer(FF name) | Load |

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clk\_in | BUFGP | 19 |

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**RTL Schematics**

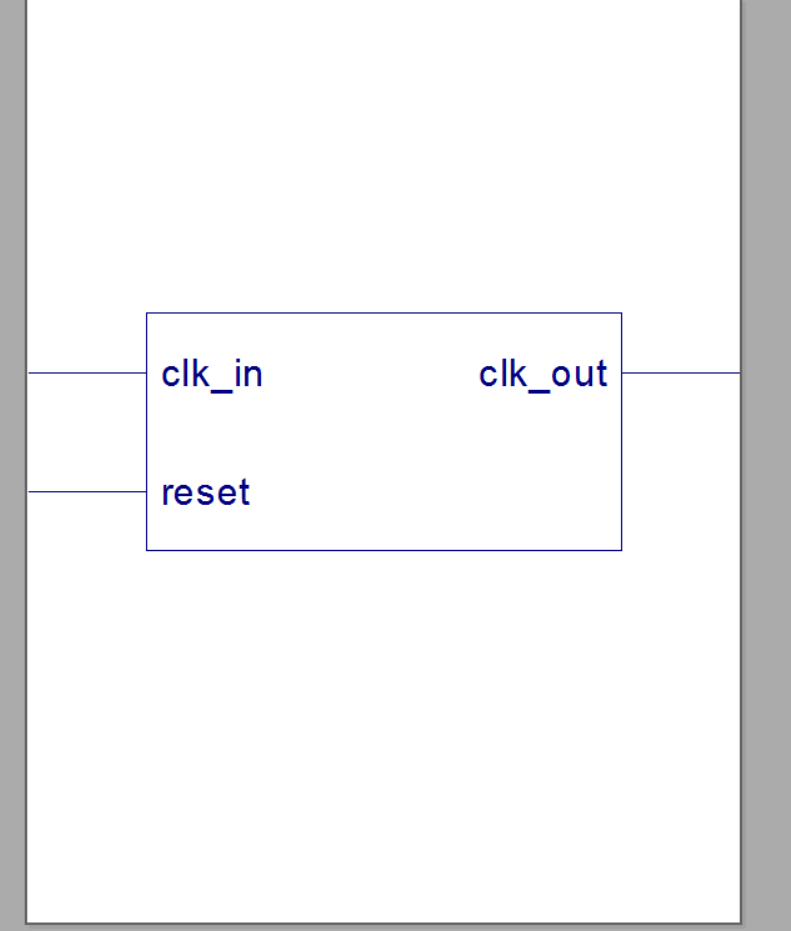
The RTL schematics of inner and outer layer are shown as below:-

Figure No-3.3.1

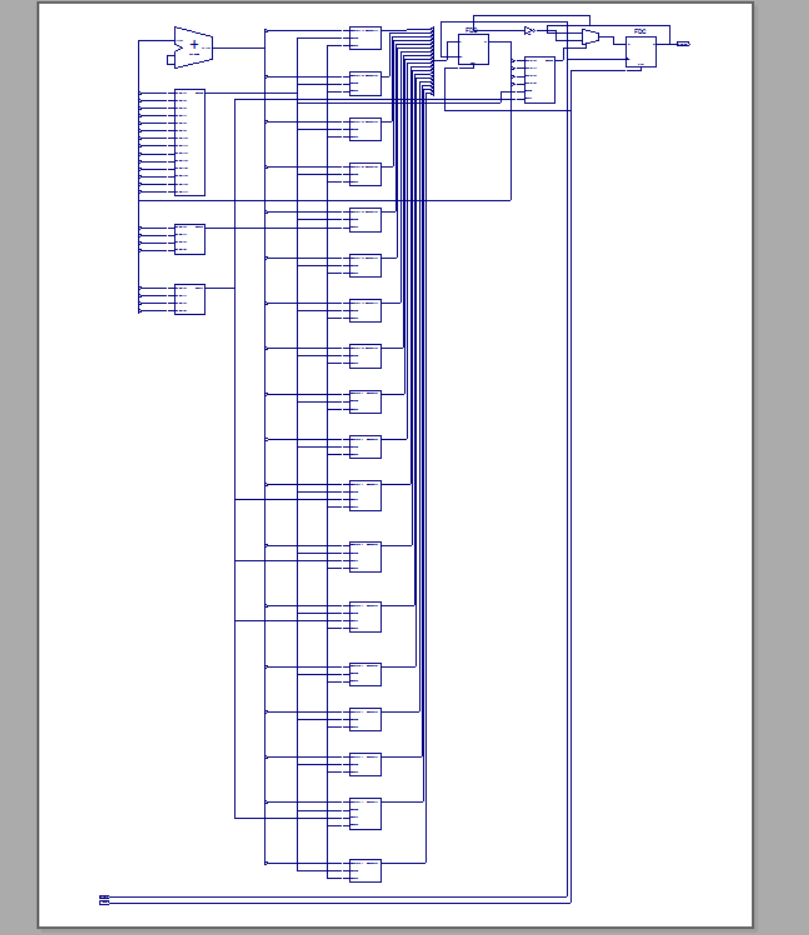
Above is the RTL schematic of the Outer layer, the black box diagram shows only the inputs and outputs. The duty cycle and dividing factor inputs have been hardcoded will appear in the final schematic.

Figure No-3.3.2

Above is the RTL schematic of the inner layer. The RTL schematic is obtained using the In-built option in Xilinx IDE. As a result we obtain The RTL schematic and it can be depicted in two layers, the former being a Black box layer.

* 1. **Simulation, Waveform and Results.**

The simulation was carried out using Model-Sim software. The version is Special Edition, 6.3E.

The test-bench mentioned earlier was built and run in the Model-Sim software to obtain the waveforms. As it can be seen from the waveform, the output clock signal is not only scaled down, but also the duty cycle is reduced.

The first signal is a clock signal with the frequency of 50MHz. The clock frequency is applied using a process within the test-bench.

The second signal is the reset signal, the circuit will be reset after the signal is 1, i.e. the counter will begin after reset is switched from 1 to 0.

The third signal is the output clock signal, in which we can observe that the duty cycle is 10%. The duty cycle can be changed by hard coding the value in the program directly. Further addendums will allow us to set the duty cycle using a signal within the entity.

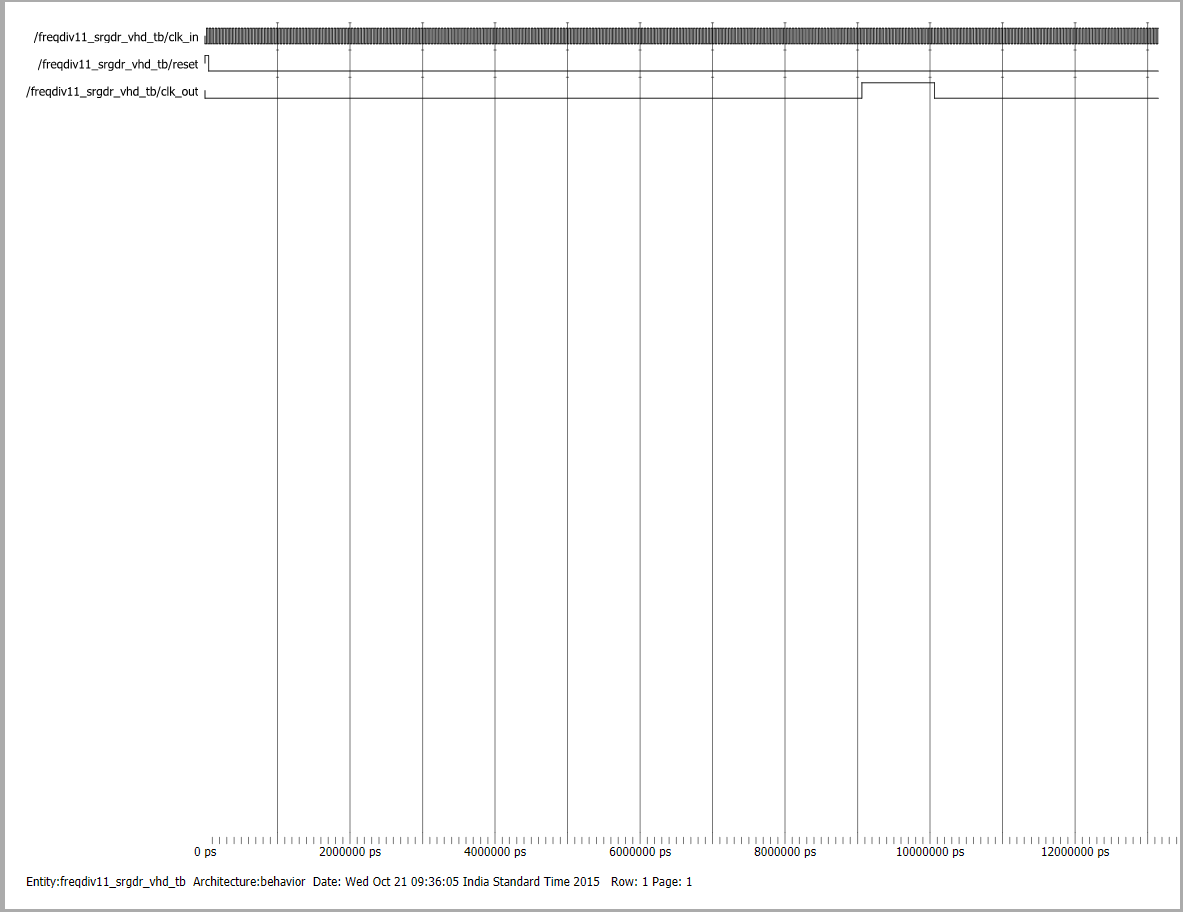


Figure No-3.4.1

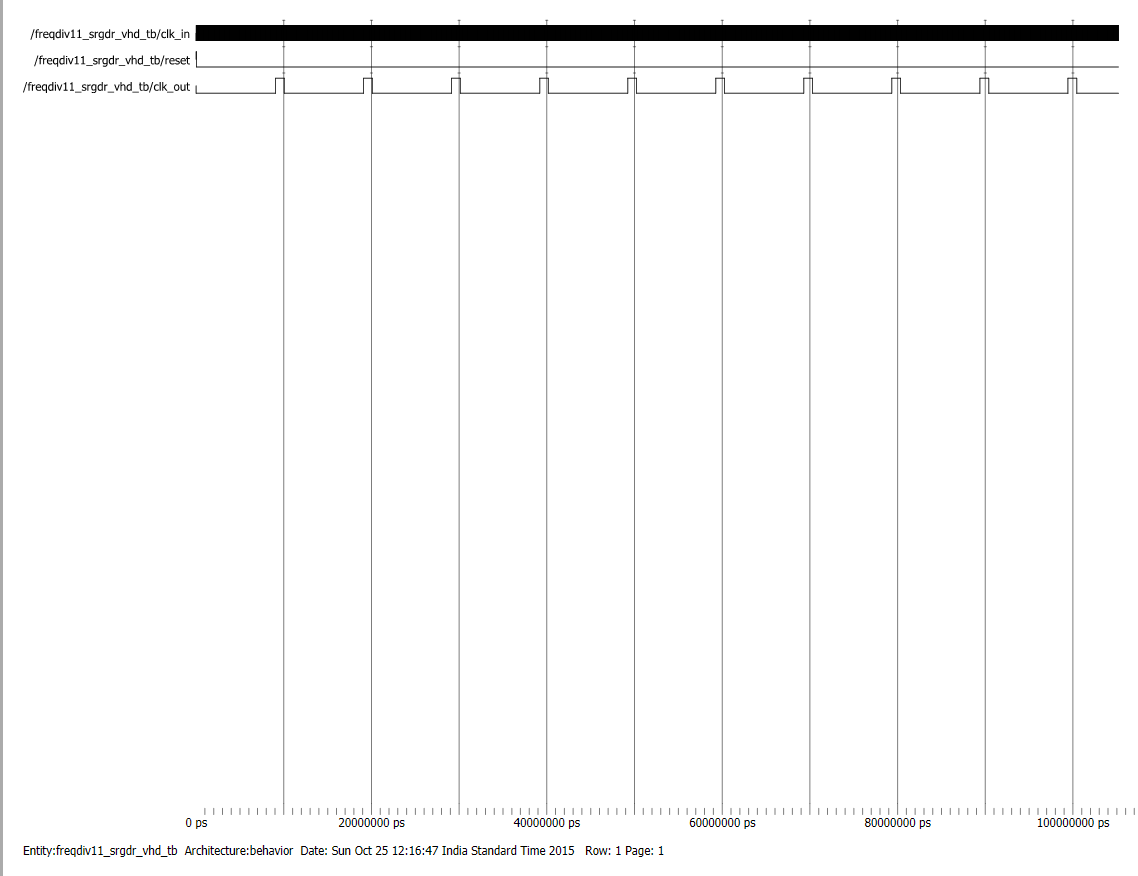


Figure No -3.4.2